

## CLAIMS

What is claimed is:

- 1           1.     A method for designing at least one mask for manufacturing an integrated  
2 circuit comprising:
  - 3                 generating a schematic for the integrated circuit, the integrated circuit  
4                 comprising a set of transistors;
  - 5                 entering data representing each transistor of the set into a computer-aided  
6                 design system;
  - 7                 identifying a first subset of the set of transistors wherein the transistors of  
8                 the first subset are expected to be subject to voltage levels beyond the bounds of a  
9                 power rail and a ground rail of the integrated circuit during normal operation;
  - 10                designating, in the computer-aided design system, robust geometries for  
11                the transistors of the first subset;
  - 12                and
  - 13                operating the computer-aided design system to generate the at least one  
14                mask.
- 1           2.     The method of claim 1 further comprising:
  - 2                 identifying a second subset of the set of transistors, wherein the transistors  
3                 of the second subset are input-output transistors
  - 4                 and
  - 5                 designating, in the computer aided design system, robust geometries for  
6                 the transistors of the second subset.

1           3.     An integrated circuit comprising:  
2                     a semiconductor die formed using at least one mask designed by the acts  
3           of:  
4                     generating a schematic for the integrated circuit, the integrated circuit  
5           comprising a set of transistors;  
6                     entering data representing each transistor of the set into a computer-aided  
7           design system;  
8                     identifying a first subset of the set of transistors wherein the transistors of  
9           the first subset are expected to be subject to voltage levels beyond the bounds of a  
10          power rail and a ground rail of the integrated circuit during normal operation;  
11          designating, in the computer-aided design system, robust geometries for  
12          the transistors of the first subset, such that the set of data may be used to generate  
13          a plurality of masks for lithography of features having mutually different  
14          minimum line widths.

1           4.     The integrated circuit claim 3 wherein:  
2                     the at least one mask is designed by acts further comprising:  
3                     identifying a second subset of the set of transistors, wherein the  
4           transistors of the second subset are input-output transistors  
5                     and  
6                     designating, in the computer aided design system, robust  
7           geometries for the transistors of the second subset.

1           5.     The integrated circuit claim 3 wherein:  
2                     the integrated circuit implements a radio frequency circuit.

1           6.     The integrated circuit claim 1 wherein:

2 the integrated circuit implements a hybrid circuit.

1 7. The integrated circuit claim 3 wherein:

2 the semiconductor die comprises metal-oxide transistors is formed using  
3 lithography.

1 8. A method for designing a plurality of masks for manufacturing an  
2 integrated circuit migrated across a plurality of feature size technologies, each mask  
3 associated with a respective feature size technology, the method comprising:

4 generating a schematic for the integrated circuit, the integrated circuit  
5 comprising a set of transistors;

6 entering data representing each transistor of the set into a computer-aided  
7 design system;

8 identifying a first subset of the set of transistors wherein the transistors of  
9 the first subset are expected to be subject to voltage levels beyond the bounds of a  
10 power rail and a ground rail of the integrated circuit during normal operation;

11 designating, in the computer-aided design system robust geometries for the  
12 transistors of the first subset;

13 and

14 operating the computer aided design system to generate a first mask  
15 associated with a first feature size technology and a second mask associated with  
16 a second feature size technology, wherein a respective geometry of each transistor  
17 of the first subset is the same for both the first mask and the second mask.